ABSTRACT

A process for forming isolation and active regions, wherein the patterning of an oxidation-barrier active stack is performed separately in the PMOS and NMOS regions. After the active stack is in place, two masking steps are used: one exposes the isolation areas on the NMOS side, for stack etch, channel-stop implant, and silicon recess etch (optional). The other masking step is exactly complementary, and performs the analogous operations on the PMOS side. After these two steps are performed (in either order), an additional nitride layer can optionally be deposited and etched to cover the sidewall of the active stack. Field oxide is then formed, and processing then proceeds in conventional fashion.

91-C-127